Docket No. 55561 (70820)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Y. Kubota et al.	CONF. NO.:	7275
U.S. SERIAL NO.:	09/775,167	EXAMINER:	S. Kumar
FILED:	February 1, 2001	GROUP:	2629
FOR:	SHIFT REGISTER CIRCUIT CAPABLE OF REDUCING CONSUMPTION OF POWER WITH REDUCED CAPACITIVE LOAD OF CLOCK SIGNAL LINE AND IMAGE DISPLAY DEVICE INCLUDING IT		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE TO OFFICE ACTION

Applicants are in receipt of the Office Action dated September 21, 2007 of the above-referenced application. Applicants respond to the Office Action as follows.

Claims 1-25 are pending in the application.

Claims 1-5, 14, and 25 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,289,518 to Nakao in view of "Applicant's Admitted Prior Art (AAPA)." The remaining claims were rejected over prior art including the Nakao reference and AAPA. These rejections are respectfully traversed.

The proposed combination of Nakao in view of AAPA does not teach or suggest a shift register circuit in which an input control signal of a transfer gate of a corresponding register block is brought into an ON-state **only** in a specified period when an output of the corresponding flip-flop **changes**.

In the "Response to Arguments" section on pages 8-9 of the Office Action of 09/21/2007, the Examiner cited the following passage on page 7, lines 6-8 of the specification, which states: "only when the output of the flip-flop of each stage of the shift register circuit is significant (in an active state), a clock signal is inputted to the flip-flop."

Regarding the above passage of the Applicants' specification, the Examiner alleged: "thus when the output is not significant then it is not in the ON state, therefore teaching where the register block is brought into an ON state when the flip flop changes."

However, independent claims 1 and 25 require that an input control signal is brought into an ON-state **only** in a specified period during which an output of a flip-flop **changes**.

The above-cited passage of the specification (page 7, lines 6-8) refers to a prior art shift register circuit depicted in FIG. 39, where signal waveforms are shown in FIGS. 40A-40J and FIGS. 41A-41J. In particular, FIGS. 41A-41J were cited on page 3, lines 1-2 of the Office Action of 09/21/2007.

For example, referring to FIGS. 41C and 41D, the signal OUT1 represents an output signal, and the signal CTL1 represents a control signal (see specification at page 8, lines 3-9). It is apparent from FIGS. 41C and 41D of the application that the control signal CTL1 is not "brought into an ON-state **only** in a specified period during which an output [OUT1] of the flip-flop of the corresponding register block **changes**" (emphasis added), as recited in independent claim 1 (*see also* claim 25).

Instead, as shown in FIGS. 41C and 41D, the control signal CTL1 remains in an ON-state during the entire period in which the output OUT1 of the flip-flop is active, and thus is not limited to the time period in which the output of the flip-flop changes, as required in independent claims 1 and 25.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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Date: December 20, 2007

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